

OGPT-24,727



PATENT

3/A
V. 24
2/16/01

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Jay B. Ross and Merle T. Proulx

Serial No.: 09/389,567

For: UNIVERSAL SERIAL BIT STREAM PROCESSOR

RECEIVED
DEC 18 2000
Technology Center 2100

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

PRELIMINARY AMENDMENT

Prior to the initial review, please amend as follows the pending application Serial No. 09/389,567 filed on September 3, 1999.

IN THE CROSS REFERENCE TO RELATED APPLICATIONS

Page 2, line 5, change "No. _____" to --No. 09/390,221--.

line 7, change "No. _____" to --No. 09/389,542--.

line 9, change "No. _____" to --No. 09/390,499--.

Page 34, line 7, change "© = D)" to --(C = D)--.

Page 38, line 5, change "1008" to --1006--.

line 6, change "1008" to --1006--.

Page 42, line 16, change "1404" to --1406--.

Page 67, line 2, change "correction" to --detection--.

Page 68, line 6, change "tot eh" to --to the--.



AMENDMENT TRANSMITTAL FORM

Attorney Docket No. OGPT-24,727

In re the Application of: Jay B. Ross and Merle T. Proulx
Serial No.: 09/389,567
Filed: September 3, 1999
Group: 2761
Examiner:
For: UNIVERSAL SERIAL BIT STREAM PROCESSOR

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THE COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Sir:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated as shown below:

CLAIMS AS AMENDED						
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE
Total Claims	20	Minus	20	0	\$ 9.00 =	\$ 00.00
Independent Claims	2	Minus	3	0	\$ 39.00 =	\$00.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						\$00.00

Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 20-0780/OGPT-24,727 of HOWISON, CHAUZA, HANDLEY & ARNOTT, L.L.P.

12/5/00
Date

Attorney for Applicant
Registration No. 30,646

IN THE DRAWINGS

Please amend Figure 1 according to the attached amended drawing by placing a connecting dot at the intersection of the lines to the right of block 112. Additionally, please amend item number 1004 of Figure 10B according to the attached amended drawing to read 1-OF-16, and not 1-TO-46, as currently marked.

IN THE CLAIMS

Please delete Claims 1-14, and insert therefor the following claims 15-34:

- Sub-
C1
of
prior art
-
15. A bit stream processor, comprising:
 a memory having one or more inputs for receiving respective input bit streams,
 said input bit streams of said one or more inputs defining a plurality of input combinations to
 said memory;
 an opcode input of said memory for inputting a selected one of one or more
 opcodes, which said selected one of said one or more opcodes operates on said input
 combinations; and
 an output of said memory for outputting an output bit stream.--
- 16. The processor of Claim 15, wherein said memory is a bit-addressable memory
 where each said input combination of said plurality of input combinations is mapped to a unique
 bit location in said memory.--
- 17. The processor of Claim 15, wherein said memory comprises binary memory
 devices which can be individually and selectively read.--
- 18. The processor of Claim 15, wherein said input combinations comprise separate
 address inputs which are selected by said select one of said one or more opcodes.--